

Application Specific Products

• Series 28

DESCRIPTION

The PLS105 is a bipolar programmable state machine of the Mealy type. It contains logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output Registers. These consist respectively of 6 Q_p, and 8 Q_f edge-triggered, clocked S/R flip-flops, with an Asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs I₀ - I₁₅ with six internal inputs P₀ - P₅, which are fed back from the State Registers to form up to 48 transition terms (AND terms). All transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low-to-High transition of the Clock pulse. Both True and Complement transition terms can be generated by optional use of the internal input variable (C) from the Complement Array. Also, if desired, the Preset input can be converted to Output Enable function, as an additional user-programmable option.

Order codes are contained on the pages following.

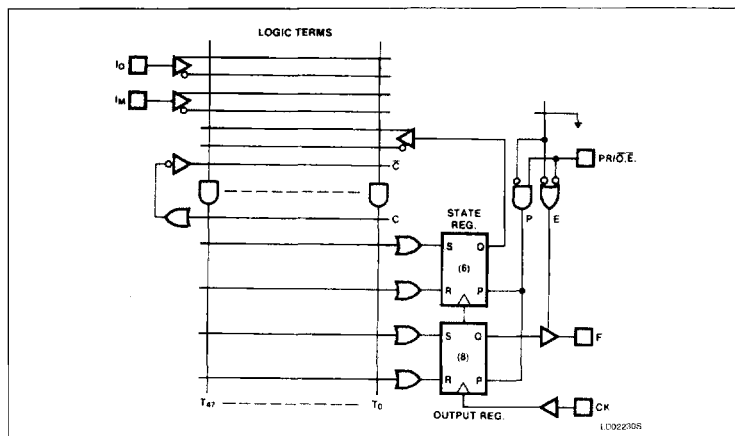
FEATURES

- Field-Programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-bit State Register
- 8-bit Output Register
- Transition Complement Array
- Positive edge-triggered clocked flip-flops
- Programmable Asynchronous Preset or Output Enable
- Power-on preset to all "1" of internal registers
- f_{MAX} = 13.9MHz
- Power dissipation: 600mW (typ.)
- TTL compatible
- Single +5V supply
- Tri-state outputs

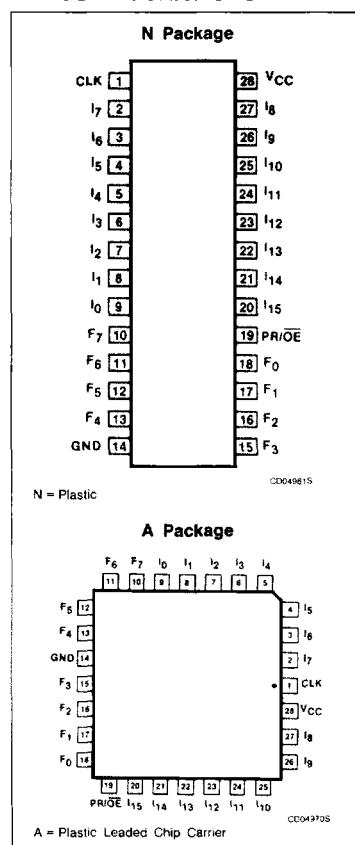
APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems
- Counters
- Shift registers

FUNCTIONAL DIAGRAM

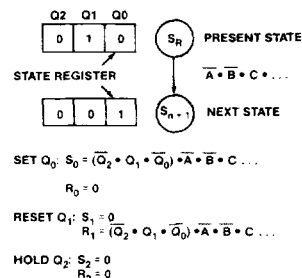


PIN CONFIGURATIONS



LOGIC FUNCTION

Typical State Transition:



Field-Programmable Logic Sequencer (16 × 48 × 8)

PLS105

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION	POLARITY
1	CK	Clock: The Clock input to the State and Output Registers. A Low-to-High transition on this line is necessary to update the contents of both registers.	Active-High
2-8 20-27	I ₁₋₁₅	Logic Inputs: The 15 external inputs to the AND array used to program jump conditions between machine states, as determined by a given logic sequence.	Active-High/Low
9	I ₀	Logic/Diagnostic Input: A 16th external logic input to the AND array, as above, when exercised with standard TTL levels. When I ₀ is held at +10V, device outputs F ₀₋₅ reflect the contents of State Register bits P ₀₋₅ . The contents of each Output Register remains unaltered.	Active-High/Low
10-13 15-18	F ₀₋₇	Logic/Diagnostic Outputs: Eight device outputs which normally reflect the contents of Output Register bits Q ₀₋₇ , when enabled. When I ₀ is held at +10V, F ₀₋₅ = (P ₀₋₅), and F _{6,7} = Logic "1".	Active-High
19	PR/ $\overline{OE}$	Preset or Output Enable Input: A user programmable function: • Preset: Provides an Asynchronous Preset to logic "1" of all State and Output Register bits. Preset overrides Clock, and when held High, clocking is inhibited and F ₀₋₇ are High. Normal clocking resumes with the first full clock pulse following a High-to-Low clock transition, after Preset goes Low. • Output Enable: Provides an Output Enable function to all output buffers F ₀₋₇ from the Output Register.	Active-High (H) Active-Low (L)

TRUTH TABLE 1, 2, 3, 4, 5, 6

V _{CC}	OPTION		I ₀	CK	S	R	Q _{p/f}	F
	PR	$\overline{OE}$						
+5V	H		*	X	X	X	H	H
	L		+10V	X	X	X	Q _n	(Q _p) _n
	L		X	X	X	X	Q _n	(Q _f) _n
		H	*	X	X	X	Q _n	Hi-Z
		L	+10V	X	X	X	Q _n	(Q _p) _n
		L	X	X	X	X	Q _n	(Q _f) _n
		L	X	↑	L	L	Q _n	(Q _f) _n
		L	X	↑	L	H	L	L
		L	X	↑	H	L	H	H
		L	X	↑	H	H	IND.	IND.
↑	X	X	X	X	X	X	H	

NOTES:

- Positive Logic:
S/R = T₀ + T₁ + T₂ + ... + T₄₇
T_n = C(I₀ I₁ I₂...) (P₀ P₁...P₅)
- Either Preset (Active-High) or Output Enable (Active-Low) are available, but not both. The desired function is a user-programmable option.
- ↑ denotes transition from Low to High level.
- R = S = High is an illegal input condition.
- * = H/L/+10V
- X = Don't Care (< 5.5V)

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

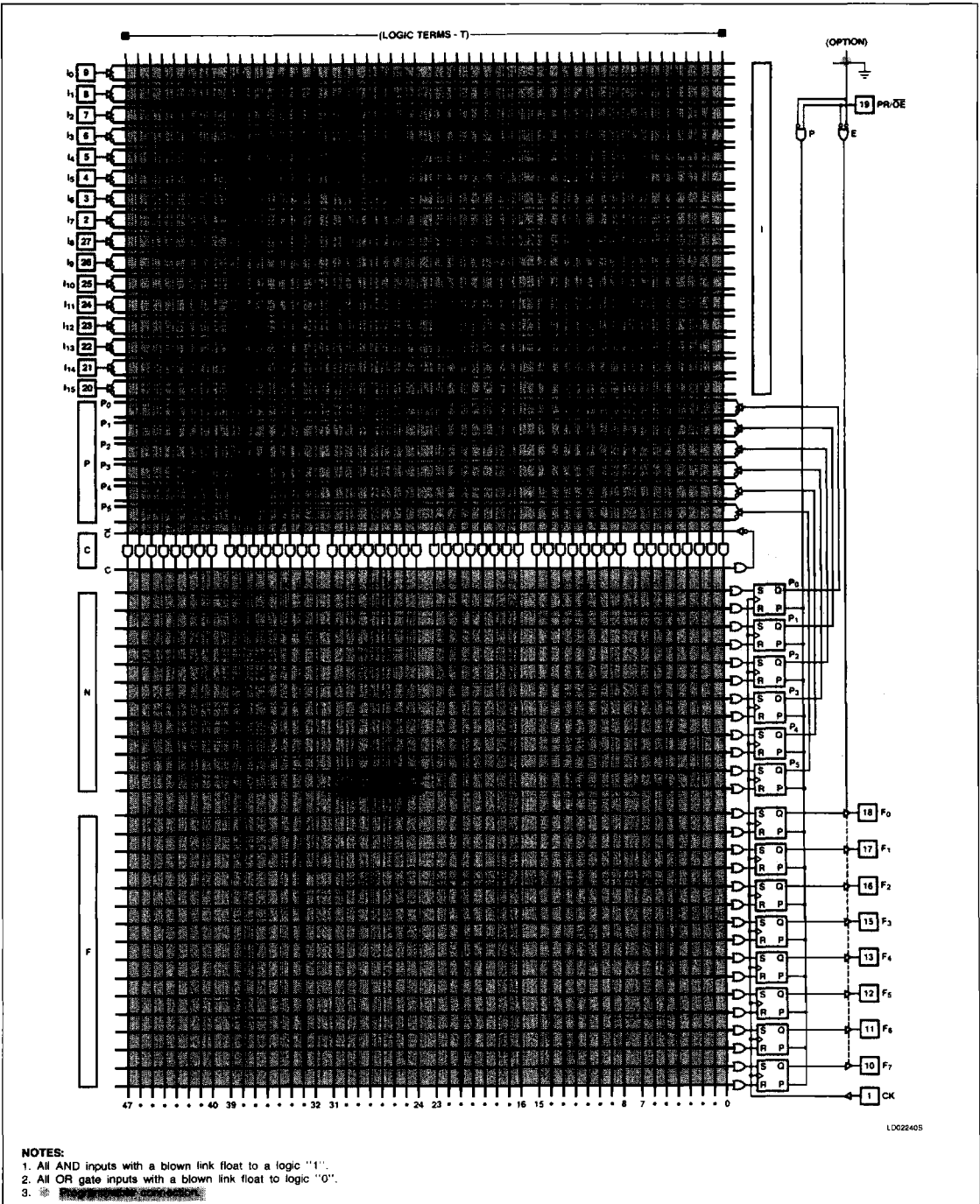
- PR/ $\overline{OE}$ option is set to PR. Thus, all outputs will be at "1", as preset by initial power-up procedure.
- All transition terms are disabled (0).
- All S/R flip-flop inputs are disabled (0).
- The device can be clocked via a Test Array pre-programmed with a standard test pattern.

NOTE: The Test Array pattern MUST be deleted before incorporating a user program. This is accomplished automatically when using Signetics qualified programming equipment.

Field-Programmable Logic Sequencer (16 × 48 × 8)

PLS105

FPLS LOGIC DIAGRAM



Field-Programmable Logic Sequencer (16 × 48 × 8)

PLS105

ORDERING INFORMATION

DESCRIPTION	ORDER CODE
28-pin Plastic DIP 600mil-wide	PLS105N
28-pin Plastic Leaded Chip Carrier	PLS105A

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V _{CC}	Supply voltage		+ 7	V _{DC}
V _{IN}	Input voltage		+ 5.5	V _{DC}
V _{OUT}	Output voltage		+ 5.5	V _{DC}
I _{IN}	Input currents	-30	+ 30	mA
I _{OUT}	Output currents		+ 100	mA
T _A T _{STG}	Temperature range Operating Storage	0 -65	+ 75 + 150	°C

DC ELECTRICAL CHARACTERISTICS 0°C ≤ T_A ≤ 75°C, 4.75V ≤ V_{CC} ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Min	Typ ²	Max	
Input voltage ³						
V _{IH} V _{IL} V _{IC}	High Low Clamp ⁴	V _{CC} = Max V _{CC} = Min V _{CC} = Min, I _{IN} = -12mA	2		0.8 -1.2	V
Output voltage ³						
V _{OH} V _{OL}	High ⁵ Low ⁶	V _{CC} = Min I _{OH} = -2mA I _{OL} = 9.6mA	2.4	0.35	0.45	V
Input current						
I _{IH} I _{IL} I _{IL}	High Low Low (CK input)	V _{IN} = 5.5V V _{IN} = 0.45V V _{IN} = 0.45V		< 1 -10 -50	25 -100 -250	μA
Output current						
I _{O(OFF)} I _{OS}	Hi-Z state ⁷ Short circuit ^{4,8}	V _{CC} = Max V _{OUT} = 5.5V V _{OUT} = 0.45V V _{OUT} = 0V		1 -1	40 -40 -70	μA mA
I _{CC}	V _{CC} supply current ⁹	V _{CC} = Max		120	180	mA
Capacitance ⁷						
C _{IN} C _{OUT}	Input Output	V _{CC} = 5.0V V _{IN} = 2.0V V _{OUT} = 2.0V		8 10		pF

See Notes on following page.

Field-Programmable Logic Sequencer (16 × 48 × 8)

PLS105

NOTES:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.
2. All typical values are at $V_{CC} = 5V$, $T_A = +25^\circ C$.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{OE}$ and a logic high stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the output is at a low logic level, and V_{IL} applied to PR/ $\overline{OE}$. Output sink current is supplied through a resistor to V_{CC} .
7. Measured with V_{IH} applied to PR/ $\overline{OE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/ $\overline{OE}$ input grounded, all other inputs at 4.5V and the outputs open.

AC ELECTRICAL CHARACTERISTICS $R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$, $0^\circ C \leq T_A \leq +75^\circ C$, $4.75V \leq V_{CC} \leq 5.25V$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ ¹	Max	
Pulse width							
t _{CKH}	Clock ² high	CK -	CK +	25	15		ns
t _{CKL}	Clock low	CK +	CK -	25	15		
t _{CKP1B}	Period (without Complement Array)	CK +	CK +	80	40		
t _{CKP2B}	Period (with Complement Array)	CK +	CK +	120	60		
t _{PRH}	Preset pulse	PR -	PR +	25	15		
Setup time ³							
t _{IS1A}	Input	CK +	Input ±	60			ns
t _{IS1B}	Input	CK +	Input ±	50			
t _{IS1C}	Input	CK +	Input ±	42			
t _{IS2A}	Input (through Complement Array)	CK +	Input ±	90			
t _{IS2B}	Input (through Complement Array)	CK +	Input	80			
t _{IS2C}	Input (through Complement Array)	CK +	Input	72			
t _{VS}	Power-on preset	CK -	V _{CC} +	0	-10		
t _{PRS}	Preset	CK -	PR -	0	-10		
Hold time							
t _{IH}	Input	Input ±	CK +	5	-10		ns
Propagation delay							
t _{CKO}	Clock	Output ±	CK +		15	30	ns
t _{OE}	Output enable	Output -	OE -		20	30	
t _{OD}	Output disable	Output +	OE +		20	30	
t _{PR}	Preset	Output +	PR +		18	30	
t _{PPR}	Power-on preset	Output +	V _{CC} +		0	10	
Frequency of operation ³							
f _{MAXC}	Without Complement Array					13.9	MHz
f _{MAXC}	With Complement Array					9.8	

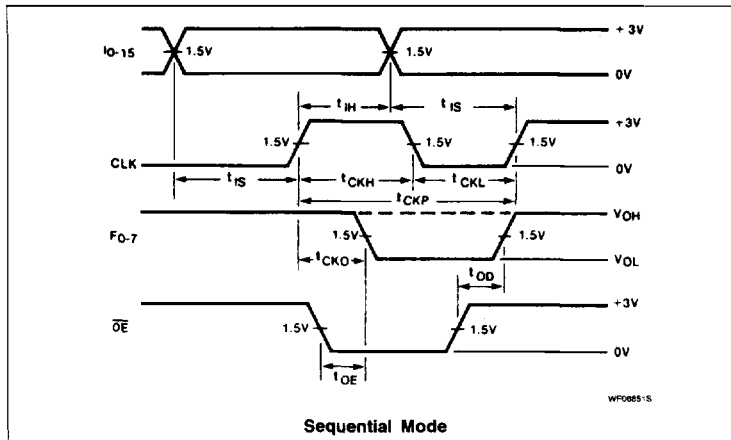
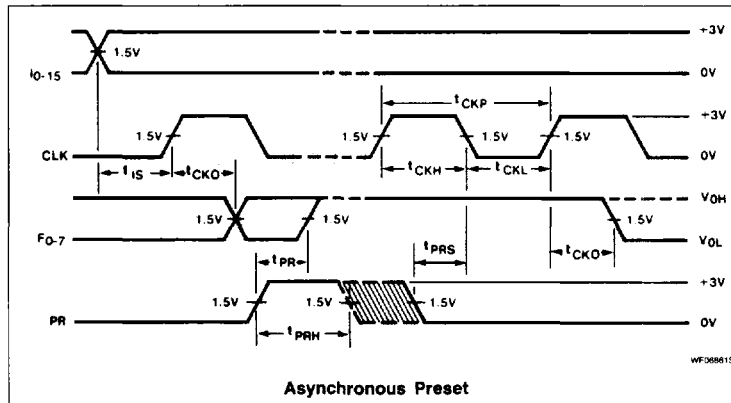
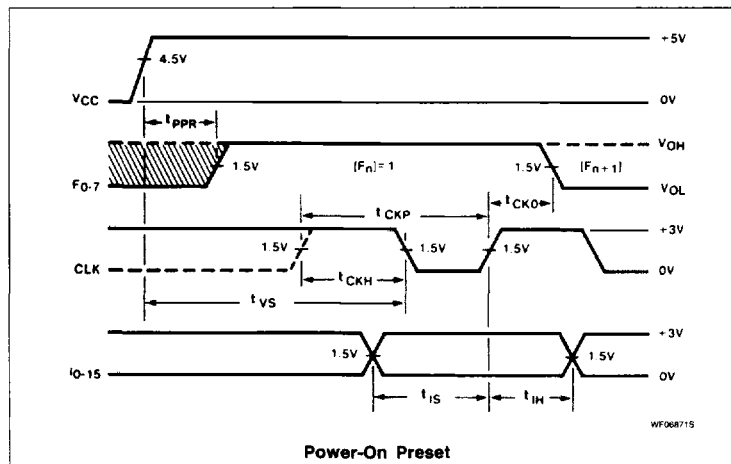
NOTES:

1. All typical values are at $V_{CC} = 5V$, $T_A = +25^\circ C$.
2. To prevent spurious clocking, clock rise time (10% - 90%) $\leq 30ns$.
3. See "Speed vs. OR Loading" diagrams.

Field-Programmable Logic Sequencer (16 × 48 × 8)

PLS105

TIMING DIAGRAMS



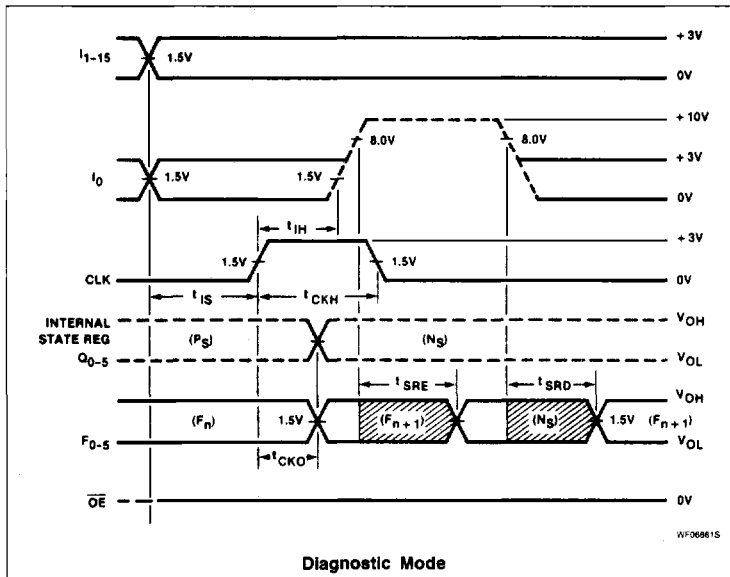
TIMING DEFINITIONS

- t_{CKH} Width of input clock pulse.
 t_{CKL} Interval between clock pulses.
 t_{CKP1} Clock period - when not using Complement Array.
 t_{IS1} Required delay between beginning of valid input and positive transition of Clock.
 t_{CKP2} Clock period - when using Complement Array.
 t_{IS2} Required delay between beginning of valid input and positive transition of Clock, when using optional Complement Array (two passes necessary through the AND Array).
 t_{VS} Required delay between V_{CC} (after power-on) and negative transition of Clock preceding first reliable clock pulse.
 t_{PRS} Required delay between negative transition of Asynchronous Preset and negative transition of Clock preceding first reliable clock pulse.
 t_{IH} Required delay between positive transition of Clock and end of valid Input data.
 t_{CKO} Delay between positive transition of clock and when outputs become valid (with PR/ $\overline{OE}$ low).
 t_{OE} Delay between beginning of Output Enable Low and when Outputs become valid.
 t_{OD} Delay between beginning of Output Enable High and when Outputs are in the off state.
 t_{SRE} Delay between input I_0 transition to Diagnostic Mode and when the Outputs reflect the contents of the State Register.
 t_{SRD} Delay between input I_0 transition to Logic mode and when the Outputs reflect the contents of the Output Register.
 t_{PR} Delay between positive transition of Preset and when Outputs become valid at "1".
 t_{PPR} Delay between V_{CC} (after power-on) and when Outputs become preset at "1".
 t_{PRH} Width of preset input pulse.
 f_{MAX} Maximum clock frequency.

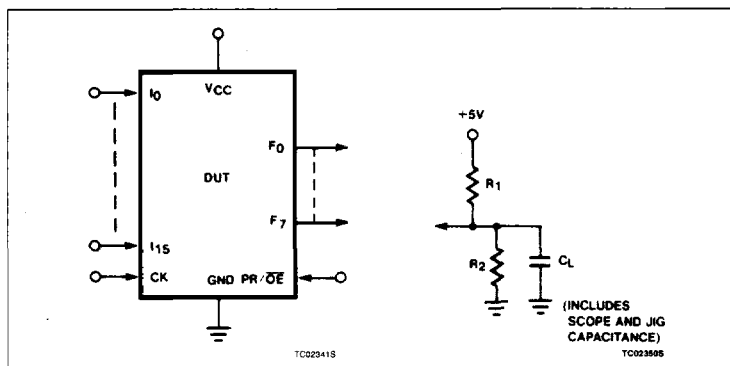
Field-Programmable Logic Sequencer ($16 \times 48 \times 8$)

PLS105

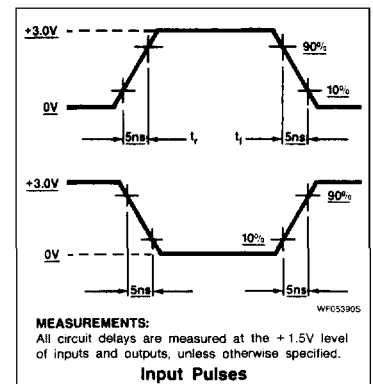
TIMING DIAGRAMS (Continued)



TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Field-Programmable Logic Sequencer (16 × 48 × 8)

PLS105

SPEED VS. "OR" LOADING

The maximum frequency at which the FPLS can be clocked while operating in *sequential mode* is given by:

$$(1/f_{MAX}) = t_{CY} = t_{IS} + t_{CKO}$$

This frequency depends on the number of transition terms T_n used. Having all 48 terms connected in the AND array does not appreciably impact performance; but the number of terms connected to each OR line affects t_{IS} , due to capacitive loading. The effect of this loading can be seen in Figure 1, showing the variation of t_{IS1} with the number of terms connected per OR.

The AC electrical characteristics contain three limits for the parameters t_{IS1} and t_{IS2} . The first, t_{IS1A} is guaranteed for a device with 48 terms connected to any OR line. t_{IS1B} is guaranteed for a device with 32 terms connected to any OR line. And t_{IS1C} is guaranteed for a device with 24 terms connected to any OR line.

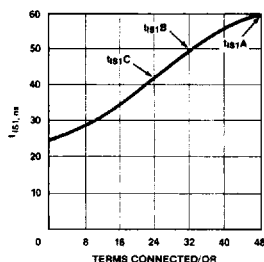


Figure 1. t_{IS1} vs. Terms/OR Connected

The three other entries in the AC table, t_{IS2} A, B, and C are corresponding 48, 32, and 24 term limits when using the on-chip Complement Array.

The worst case t_{IS} for a given application can be determined by identifying the OR line with the maximum number of T_n connections. This can be done by referring to

the interconnect pattern in the FPLS logic diagram, typically illustrated in Figure 2, or by counting the maximum number of "H" or "L" entries in one of the columns of the device Program Table.

This number plotted on the curve in Figure 1 will yield the worst case t_{IS} and, by implication, the maximum clocking frequency for reliable operation.

Note that for maximum speed all UNUSED transition terms should be disconnected from the OR array.

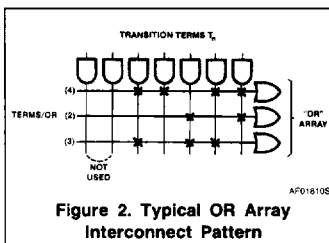


Figure 2. Typical OR Array Interconnect Pattern

Field-Programmable Logic Sequencer (16 × 48 × 8)

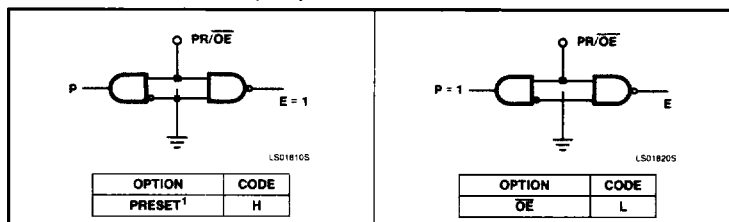
PLS105

LOGIC PROGRAMMING

The FPLS can be programmed by means of Logic programming equipment.

With Logic programming, the AND/OR gate input connections necessary to implement the desired logic function are coded directly from the State Diagram using the Program Table on the following page.

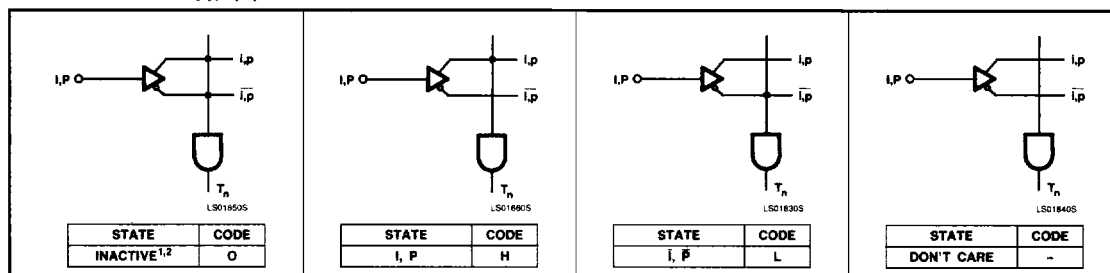
In this Table, the logic state or action of control variables C, I, P, N, and F, associated with each Transition Term T_n , is assigned a symbol which results in the proper fusing pattern of corresponding links, defined as follows:

PRESET/ $\overline{OE}$ OPTION - (P/E)

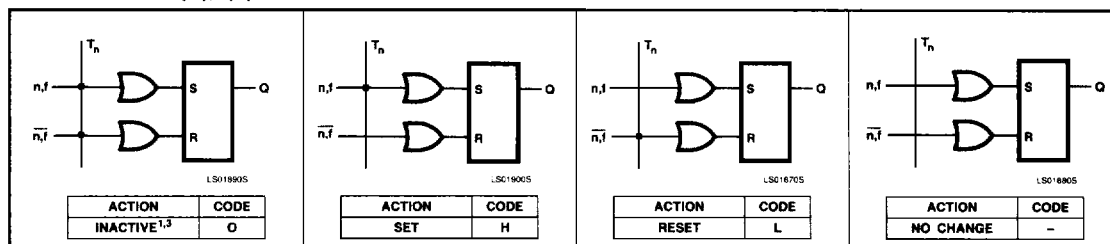
PROGRAMMING THE PLS105:

The PLS105 has a power-up preset feature. This feature insures that the device will power-up in a known state with all register elements (state and output register) at a logic High (H). When programming the device it is important to realize this is the initial state of the device. You *must* provide a next state jump if you do not wish to use all Highs (H) as the present state.

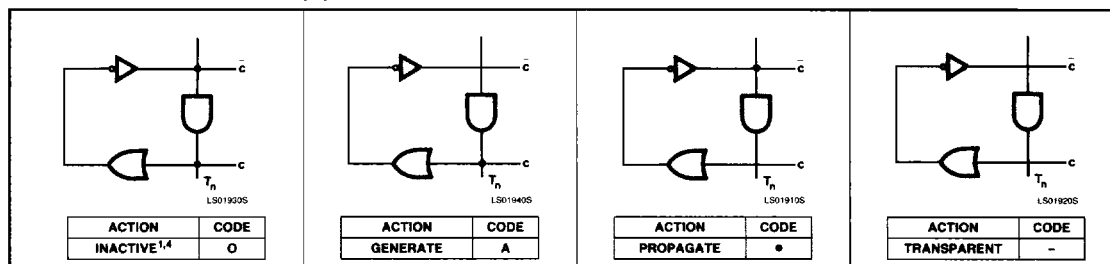
"AND" ARRAY - (I), (P)



"OR" ARRAY - (N), (F)



"COMPLEMENT" ARRAY - (C)



NOTES:

1. This is the initial unprogrammed state of all links.
2. Any gate T_n will be unconditionally inhibited if both the true and complement fuses of any input (I,P) are left intact.
3. To prevent simultaneous Set and Reset flip-flop commands, this state is not allowed for N and F link pairs coupled to active gates T_n (see flip-flop truth tables).
4. To prevent oscillations, this state is not allowed for C link pairs coupled to active gates T_n .

Field-Programmable Logic Sequencer (16 × 48 × 8)

PLS105

FPLS PROGRAM TABLE

PROGRAM TABLE ENTRIES

CUSTOMER NAME _____ PURCHASE ORDER # _____ SIGNETICS DEVICE # _____ CF (XXXX) _____ CUSTOMER SYMBOLIZED PART # _____ TOTAL NUMBER OF PARTS _____ PROGRAM TABLE _____ REV _____ DATE _____		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2" style="text-align: center;">AND</th> <th rowspan="5" style="width: 10%; text-align: center; vertical-align: middle;">Cn</th> <th colspan="2" style="text-align: center;">OR</th> <th rowspan="5" style="width: 10%; text-align: center; vertical-align: middle;">Ns, Fr</th> </tr> <tr> <td style="width: 15%;">INACTIVE</td> <td style="width: 15%;">0</td> <td style="width: 15%;">INACTIVE</td> <td style="width: 15%;">0</td> </tr> <tr> <td>GENERATE</td> <td>A</td> <td>SET</td> <td>H</td> </tr> <tr> <td>PROPAGATE</td> <td>0</td> <td>RESET</td> <td>L</td> </tr> <tr> <td>TRANSPARENT</td> <td>—</td> <td>NO CHANGE</td> <td>—</td> </tr> </table> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th colspan="2" style="text-align: center;">OPTION</th> <th rowspan="3" style="width: 10%; text-align: center; vertical-align: middle;">Im, Ps</th> <th colspan="2" style="text-align: center;">OPTION</th> <th rowspan="3" style="width: 10%; text-align: center; vertical-align: middle;">P/E</th> </tr> <tr> <td style="width: 15%;">INACTIVE</td> <td style="width: 15%;">0</td> <td style="width: 15%;">PRESET</td> <td style="width: 15%;">H</td> </tr> <tr> <td>I, P</td> <td>H</td> <td>OE</td> <td>L</td> </tr> <tr> <td>I, F</td> <td>L</td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>DON'T CARE</td> <td>—</td> <td></td> <td></td> <td></td> <td></td> </tr> </table>		AND		Cn	OR		Ns, Fr	INACTIVE	0	INACTIVE	0	GENERATE	A	SET	H	PROPAGATE	0	RESET	L	TRANSPARENT	—	NO CHANGE	—	OPTION		Im, Ps	OPTION		P/E	INACTIVE	0	PRESET	H	I, P	H	OE	L	I, F	L					DON'T CARE	—				
AND		Cn	OR		Ns, Fr																																														
INACTIVE	0		INACTIVE	0																																															
GENERATE	A		SET	H																																															
PROPAGATE	0		RESET	L																																															
TRANSPARENT	—		NO CHANGE	—																																															
OPTION		Im, Ps	OPTION		P/E																																														
INACTIVE	0		PRESET	H																																															
I, P	H		OE	L																																															
I, F	L																																																		
DON'T CARE	—																																																		

AND		OPTION (P/E)				
OR		OR				
T E R M	Cn	INPUT (Im)	PRESENT STATE (Ps)	REMARKS	NEXT STATE (Ns)	OUTPUT (Fr)
		5 4 3 2 1 0	5 4 3 2 1 0		5 4 3 2 1 0	5 4 3 2 1 0
0						
1						
2						
3						
4						
5						
6						
7						
8						
9						
10						
11						
12						
13						
14						
15						
16						
17						
18						
19						
20						
21						
22						
23						
24						
25						
26						
27						
28						
29						
30						
31						
32						
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						
43						
44						
45						
46						
47						

PIN NO.	2	3	4	5	6	7	8	9
0	2	3	4	5	6	7	8	9
1	2	3	4	5	6	7	8	9
2	2	3	4	5	6	7	8	9
3	2	3	4	5	6	7	8	9
4	2	3	4	5	6	7	8	9
5	2	3	4	5	6	7	8	9
6	2	3	4	5	6	7	8	9
7	2	3	4	5	6	7	8	9
8	2	3	4	5	6	7	8	9
9	2	3	4	5	6	7	8	9

VARIABLE NAME	1	2	3	4	5	6	7	8	9
0	1	2	3	4	5	6	7	8	9
1	1	2	3	4	5	6	7	8	9
2	1	2	3	4	5	6	7	8	9

6

NOTES:

- NOTES
1. The FPLS is shipped with all links initially intact. Thus, a background of "0" for all Terms, and an "H" for the P/E option, exits in the table, shown BLANK instead for clarity.
 2. Unused Cn, Im, and Ps bits are normally programmed Don't Care (-).
 3. Unused Transition Terms can be left blank for future code modification, or programmed as (-) for maximum speed.
 4. Letters in variable fields are used as identifiers by logic type programmed.

LD022515

Field-Programmable Logic Sequencer (16 × 48 × 8)

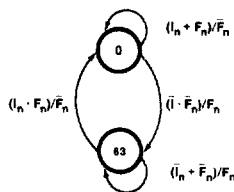
PLS105

TEST ARRAY

The FPLS may be subjected to AC and DC parametric tests prior to programming via an on-chip test array.

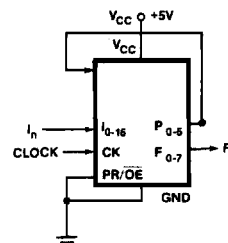
The array consists of test transition terms 48 and 49, factory programmed as shown below.

Testing is accomplished by clocking the FPLS and applying the proper input sequence to I_{0-15} as shown in the test circuit timing diagram.



State Diagram

APC18205



FPLS Under Test

TCD15975

TEST ARRAY PROGRAM

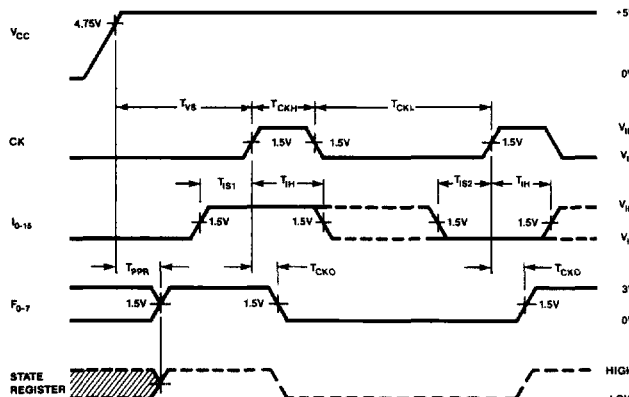
T E R M	C	AND																PRESENT STATE (P _n)															
		INPUT (I _m)																															
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	5	4	3	2	1	0	5	4	3	2	1	0			
48	A	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H				
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L				

OPTION (P/E)																H													
OR																													
NEXT STATE (N_n)																OUTPUT (F_f)													
5	4	3	2	1	0	7	6	5	4	3	2	1	0			L	L	L	L	L	L	L	L	L	L	L	L	L	L
H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

TBD17805

Test Array Program

Both terms 48 and 49 must be deleted during user programming to avoid interfering with the desired logic function. This is accomplished automatically by any of Signetics' qualified programming equipment.



Test Circuit Timing Diagram

WF03275

TEST ARRAY DELETED

T E R M	AND																												
	C	INPUT (Im)																PRESENT STATE (Ps)											
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	5	4	3	2	1	0	5	4	3	2	1	0
48	—	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
49	●	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L

OPTION (P/E)																H													
OR																													
NEXT STATE (N_n)																OUTPUT (F_f)													
5	4	3	2	1	0	7	6	5	4	3	2	1	0			—	—	—	—	—	—	—	—	—	—	—	—	—	—
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

TBD17505

Test Array Deleted